IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.:5782
Mulder *et al.*	Art Unit: 2816
Appl. No.: To Be Assigned *(Cont. of Appl. No.: 10/158,193; Filed: May 31, 2002)*	Examiner: To Be Assigned
Filed: Herewith (November 25, 2003)	Atty. Docket: 1875.2800001/RES/GSB
For: **Class AB Digital to Analog Converter/Line Driver**	

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not

be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was

first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

□ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

□ c. Attached is our PTO-2038 Credit Card Payment Form [OR] Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p).

□ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Attached is our PTO-2038 Credit Card Payment Form [OR] Check No. _____ in the amount of $ _____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

□ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

□ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more

than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below:

☒ 7. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 10/158,193, filed May 31, 2003, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

George S. Bardmesser
Attorney for Applicants
Registration No. 44,020

Date: 11/25/03

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Washington, D.C. 20005-3934
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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.2800001	APPLICATION NO. *To Be Assigned*
	APPLICANT Mulder *et al.*	
	FILING DATE *Herewith*	GROUP *To Be Assigned*

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	6,259,745 B1	07/2001	Chan	375	285	
	AB1	5,554,943	09/1996	Moreland	327	65	
	AC1	5,118,971	06/1992	Schenck	326	32	
	AD1	5,006,727	04/1991	Ragosch et al.	327	65	
	AE1	4,959,563	09/1990	Schenck	326	32	
	AF1	3,846,712	11/1974	Kiko	330	30	
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 5, May 1999, pp. 599-606.
	AS	1	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.
	AT	1	Bult, Klaas and Buchwald, Aaron, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm²," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pp. 1887-1895.

EXAMINER	DATE CONSIDERED

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	AA2						
	AB2						
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	2	Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 3, March 1995, pp. 166-172.
	AS	2	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1781-1790.
	AT	2	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 12, December 2001, pp. 1847-1858.

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	AA3						
	AB3						
	AC3						
	AD3						
	AE3						
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	AH3						
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	AJ3						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pp. 1932-1938.
	AS	3	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," IEEE International Solid-State Circuits Conference, IEEE, 2001, pp. 128-129 and 438.
	AT	3	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm², " *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1796-1802.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						
	AK4						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	4	Hosotani, S. et al., "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 25, No. 1, February 1990, pp. 167-172.
	AS	4	Ingino, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.
	AT	4	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5						
	AB5						
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	AJ5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	5	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," *IEEE International Solid-State Conference*, IEEE, 1991, pp. 170-171.
	AS	5	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.
	AT	5	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.

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	AA6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.
	AS	6	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.
	AT	6	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1760-1768.

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	AA7						
	AB7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	7	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pp. 1302-1308.
	AS	7	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1769-1780.
	AT	7	Song, W-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 5, May 1995, pp. 514-521.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	8	Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 7, July 2001, pp. 1048-1055.
	AS	8	Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.
	AT	8	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b 25-Msample/s Two-Step ADC in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1803-1811.

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	AA9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No
	AO9						Yes No
	AP9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	9	van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25-μm CMOS ADC in 1-mm^2 With Mixed-Signal Chopping and Calibration," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 12, December 2001, pp. 1859-1867.
	AS	9	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.
	AT	9	Wang, Y-T. and Razavi, B., "An 8-bit 150-MHz CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pp. 308-317.

EXAMINER	DATE CONSIDERED

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U.S. PATENT DOCUMENTS

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	AA10						
	AB10						
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	AJ10						
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FOREIGN PATENT DOCUMENTS

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	AL10						Yes No
	AM10						Yes No
	AN10						Yes No
	AO10						Yes No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	10	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pp. 1533-1537.
	AS	10	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.
	AT	10	Miyazaki *et al.*,"A 16mW 30MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture", *ISSCC 2002/Session 10/High-Speed ADCs/10.5*, February 5, 2002, 3 pgs.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
	AC11						
	AD11						
	AE11						
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	AJ11						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	11	Sushihara *et al.*, "A 7b 450MSample/s 50mW CMOS ADC in 0.3 mm^2", *ISSCC 2002/Session 10/High-Speed ADCs/10.3*, February 5, 2002, 3 pgs.
	AS	11	Dingwall *et al.*,"An 8-MHz CMOS Subranging 8-Bit A/D Converter", *IEEE Journal of Solid-State Circuits*, Vol. SC-20, No. 6, December 1985, pp. 1138-1143.
	AT	11	

EXAMINER	DATE CONSIDERED

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